XAUI PHY IP Core 7

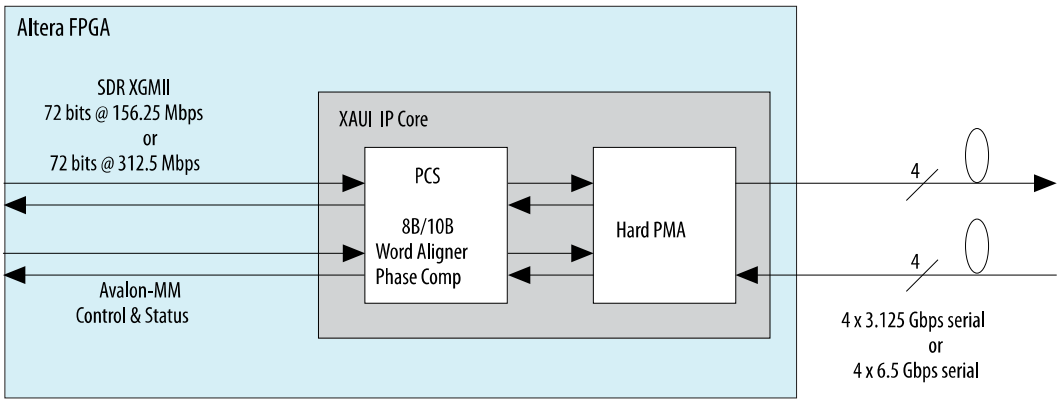
2019.02.08

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The Altera XAUI PHY IP Core implements the IEEE 802.3 Clause 48 specification to extend the operational distance of the XGMII interface and reduce the number of interface signals.

XAUI extends the physical separation possible between the 10 Gbps Ethernet MAC function and the Ethernet standard PHY component to one meter. The XAUI IP Core accepts 72-bit data (single data rate–SDR XGMII) from the application layer at either 156.25 Mbps or 312.5 Mbps. The serial interface runs at either 4 × 3.125 Gbps or 4 × 6.25 Gbps (DDR XAUI option).

Figure 7-1: XAUI PHY IP Core



For Stratix IV GX and GT devices, you can choose a hard XAUI physical coding sublayer (PCS) and physical media attachment (PMA), or a soft XAUI PCS and PMA in low latency mode. You can also combine both hard and soft PCS configurations in the same device, using all channels in a transceiver bank. The PCS is only available in soft logic for Stratix V devices.

For more detailed information about the XAUI transceiver channel datapath, clocking, and channel placement, refer to the "*XAUI*" section in the *Transceiver Configurations in Stratix V Devices* chapter of the *Stratix V Device Handbook*.

Related Information

- **IEEE 802.3 Clause 48**
- **Transceiver Configurations in Stratix V Devices**

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XAUI PHY Release Information

This section provides information about this release of the XAUI PHY IP Core.

Table 7-1: XAUI Release Information

Item	Description
Version	13.1
Release Date	November 2013
Ordering Codes[4]	P-XAUIPCS (primary)–Soft PCS IPR-XAUIPCS (renewal)–Soft PCS
Product ID	00D7
Vendor ID	6AF7

XAUI PHY Device Family Support

This section describes device family support for the IP core.

IP cores provide either final or preliminary support for target Altera device families. These terms have the following definitions:

- Final support—Verified with final timing models for this device.

Preliminary support—Verified with preliminary timing models for this device.

Table 7-2: Device Family Support

Device Family	Support
XAUI	
Arria II GX -Hard PCS and PMA	Final
Arria II GZ-Hard PCS and PMA	Final
Arria V GX-Soft PCS + PMA	Final
Arria V SoC-Soft PCS + PMA	Final
Arria V GZ devices-Soft PCS + PMA	Final
Cyclone IV GX-Hard PCS and PMA	Final
Cyclone V-Soft PCS + PMA	Final
Cyclone V SoC-Soft PCS + hard PMA	Final

[4] No ordering codes or license files are required for the hard PCS and PMA PHY in Arria II GX, Cyclone IV GX, or Stratix IV GX or GT devices.

Device Family	Support
HardCopy® IV	Final
Stratix IV GX and GT devices-Soft or hard PCS and PMA	Final
Stratix V devices-Soft PCS + PMA	Final
Other device families	No support
DXAUI	
Stratix IV GX and GT	Final
Other device families	No support

XAUI PHY Performance and Resource Utilization for Stratix IV Devices

This section describes performance and resource utilization for Stratix IV Devices

The following table shows the typical expected device resource utilization for different configurations using the current version of the Intel Quartus Prime software targeting a Stratix IV GX (EP4SG230KF40C2ES) device. The numbers of combinational ALUTs, logic registers, and memory bits are rounded to the nearest 100.

Table 7-3: XAUI PHY Performance and Resource Utilization—Stratix IV GX Device

Implementation	Number of 3.125 Gbps Channels	Combinational ALUTS	Dedicated Logic Registers	Memory Bits
Soft XAUI	4	4500	3200	5100
Hard XAUI	4	2000	1300	0

XAUI PHY Performance and Resource Utilization for Arria V GZ and Stratix V Devices

This section describes performance and resource utilization for Arria V GZ and Stratix V Devices.

For the Arria V GZ (5AGZME5K2F40C3) device, the XAUI PHY uses 1% of ALMs and less than 1% of M20K memory, primary and secondary logic registers. Resource utilization is similar for Stratix V devices.

Parameterizing the XAUI PHY

Complete the following steps to configure the XAUI PHY IP Core:

1. Under **Tools** > **IP Catalog**, select the device family of your choice.
2. Under **Tools** > **IP Catalog** > **Interfaces** > **Ethernet** select **XAUI PHY**.
3. Use the tabs on the MegaWizard Plug-In Manager to select the options required for the protocol.
4. Refer the following topics to learn more about the parameters:

a. General Parameters
b. Analog Parameters
c. Advanced Options Parameters

5. Click **Finish** to generate your customized XAUI PHY IP Core.

XAUI PHY General Parameters

This section describes the settings available on **General Options** tab.

Table 7-4: General Options

Name	Value	Description
Device family	**Arria II GX** **Arria V** **Arria V GZ** **Cyclone IV GX** **Cyclone V** **HardCopy IV** **Stratix IV** **Stratix V**	The target device family.
Starting channel number	**0-124**	The physical starting channel number in the Altera device for channel 0 of this XAUI PHY. In Arria II GX, Cyclone IV GX, HardCopy IV, and Stratix IV devices, this starting channel number must be 0 or a multiple of 4. In Arria V GZ and Stratix V devices, logical lane 0 should be assigned to either physical transceiver channel 1 or channel 4 of a transceiver bank. However, if you have already created a PCB with a different lane assignment for logical lane 0, you can use the workaound shown in **Example 7-1** to remove this restriction. Assignment of the starting channel number is required for serial transceiver dynamic reconfiguration. Check logical channel 0 restrictions in Cyclone 5 and Arria 5.

Name	Value	Description
XAUI interface type	**Hard XAUI** **Soft XAUI** **DDR XAUII**	The following 3 interface types are available: • **Hard XAUI**–Implements the PCS and PMA in hard logic. Available for Arria II, Cyclone IV, HardCopy IV, and Stratix IV devices. • **Soft XAUI**–Implements the PCS in soft logic and the PMA in hard logic. Available for HardCopy IV, Stratix IV, Arria V, Cyclone V, and Stratix V devices. • **DDR XAUI**–Implements the PCS in soft logic and the PMA in hard logic. Both the application and serial interfaces run at twice the frequency of the Soft XAUI options. Available for HardCopy IV Stratix IV devices. All interface types include 4 channels.
Data rate	Device Dependent	Specifies the data rate.
PLL type	CMU ATX	You can select either the CMU or ATX PLL. The CMU PLL has a larger frequency range than the ATX PLL. The ATX PLL is designed to improve jitter performance and achieves lower channel-to-channel skew; however, it supports a narrower range of data rates and reference clock frequencies. Another advantage of the ATX PLL is that it does not use a transceiver channel, while the CMU PLL does. This parameter is available for the soft PCS and DDR XAUI. The ATX PLL is not available for all devices.
Base data rate	1 × **Lane rate** 2 × **Lane rate** 4 × **Lane rate**	The **base data rate** is the frequency of the clock input to the PLL. Select a **base data rate** that minimizes the number of PLLs required to generate all the clock s required for data transmission. By selecting an appropriate **base data rate**, you can change data rates by changing the divider used by the clock generation block. This parameter is available for Stratix V devices.
Number of XAUI interfaces	1	Specifies the number of XAUI interfaces. Only 1 is available in the current release.

Example 7-1 shows how to remove the restriction on logical lane 0 channel assignment in Stratix V devices by redefining the pma_bonding_master parameter using the Intel Quartus Prime Assignment

Editor. In this example, the pma_bonding_master was originally assigned to physical channel 1. (The original assignment could also have been to physical channel 4.) The to parameter reassigns the pma_bonding_master to the XAUI instance name shown in quotation marks. You must substitute the instance name from your design for the instance name shown in quotation marks

Example 7-1: Overriding Logical Lane 0 Channel Assignment Restrictions in Stratix V Devices

```
set_parameter -name pma_bonding_master "\"1\"" -to "<xaui
instance name>|sv_xcvr_xaui:alt_xaui_phy|sv_xcvr_low_latency_phy_nr:
alt_pma_0|sv_xcvr_custom_native:sv_xcvr_custom_inst|sv_xcvr_native:
gen.sv_xcvr_native_insts[0].gen_bonded_group.sv_xcvr_native_inst"
```

XAUI PHY Analog Parameters

This section describes the analog parameters for the IP core.

Click on the appropriate link to specify the analog options for your device:

- **XAUI PHY Analog Parameters for Arria II GX, Cyclone IV GX, HardCopy IV and Stratix IV Devices** on page 7-6

Related Information

- **Analog Settings for Arria V Devices** on page 20-2
- **Analog Settings for Arria V GZ Devices** on page 20-11
- **Analog Settings for Cyclone V Devices** on page 20-26
- **Analog Settings for Stratix V Devices** on page 20-35

XAUI PHY Analog Parameters for Arria II GX, Cyclone IV GX, HardCopy IV and Stratix IV Devices

This section describes parameters for the Arria II GX, Cyclone IV GX, and Stratix IV devices; specify your analog options on the **Analog Options** tab.

Table 7-5: PMA Analog Options

Name	Value	Description
Transmitter termination resistance	**OCT_85_OHMS** **OCT_100_OHMS** **OCT_120_OHMS** **OCT_150_OHMS**	Indicates the value of the termination resistor for the transmitter.
Transmitter VOD control setting	**0–7**	Sets V_{OD} for the various TX buffers.
Pre-emphasis pre-tap setting	**0–7**	Sets the amount of pre-emphasis on the TX buffer. Available for Stratix IV.

Name	Value	Description
Invert the pre-emphasis pre-tap polarity setting	**On** **Off**	Determines whether or not the pre-emphasis control signal for the pre-tap is inverted. If you turn this option on, the pre-emphasis control signal is inverted. Available for HardCopy IV and Stratix IV devices.
Pre-emphasis first post-tap setting	**0–15**	Sets the amount of pre-emphasis for the 1st post-tap.
Pre-emphasis second post-tap setting	**0–7**	Sets the amount of pre-emphasis for the 2nd post-tap. Available for HardCopy IV and Stratix IV devices.
Invert the pre-emphasis second post-tap polarity	**On** **Off**	Determines whether or not the pre-emphasis control signal for the second post-tap is inverted. If you turn this option on, the pre-emphasis control signa is inverted. Available for HardCopy IV and Stratix IV devices.
Receiver common mode voltage	Tri-state 0.82V 1.1v	Specifies the RX common mode voltage.
Receiver termination resistanc	**OCT_85_OHMS** **OCT_100_OHMS** **OCT_120_OHMS** **OCT_150_OHMS**	Indicates the value of the termination resistor for the receiver. Cyclone IV supports 100 and 150.
Receiver DC gain	**0–4**	Sets the equalization DC gain using one of the following settings: • 0–0 dB • 1–3 dB • 2–6 dB • 3–9 dB • 4–12 dB
Receiver static equalizer setting	**0–15**	This option sets the equalizer control settings. The equalizer uses a pass band filter. Specifying a low value passes low frequencies. Specifying a high value passes high frequencies. Available for HardCopy IV and Stratix IV devices.

Advanced Options Parameters

This section describes the settings available on the **Advanced Options** tab.

Table 7-6: Advanced Options

Name	Value	Description
Include control and status ports	**On/Off**	If you turn this option on, the top-level IP core include the status signals and digital resets shown in XAUI Top-Level Signals—Soft PCS and PMA and XAUI Top-Level Signals–Hard IP PCS and PMA . If you turn this option off, you can access control and status information using Avalon-MM interface to the control and status registers. The default setting is off.
External PMA control and configuration	**On/Off**	If you turn this option on, the PMA signals are brought up to the top level of the XAUI IP Core. This option is useful if your design includes multiple instantiations of the XAUI PHY IP Core. To save FPGA resources, you can instantiate the Low Latency PHY Controller and Transceiver Reconfiguration Controller IP Cores separately in your design to avoid having these IP cores instantiated in each instance of the XAUI PHY IP Core. If you turn this option off, the PMA signals remain internal to the core. The default setting is off. This option is available for Arria II GX, HardCopy IV and Stratix IV devices. In these devices, this option must be turned **On** to fit 2 hard XAUI instances in adjacent transceiver quads that share the same calibration block. In addition, the instances must share powerdown signals.
Enable rx_recovered_clk pin	**On/Off**	When you turn this option on, the RX recovered clock signal is an output signal.

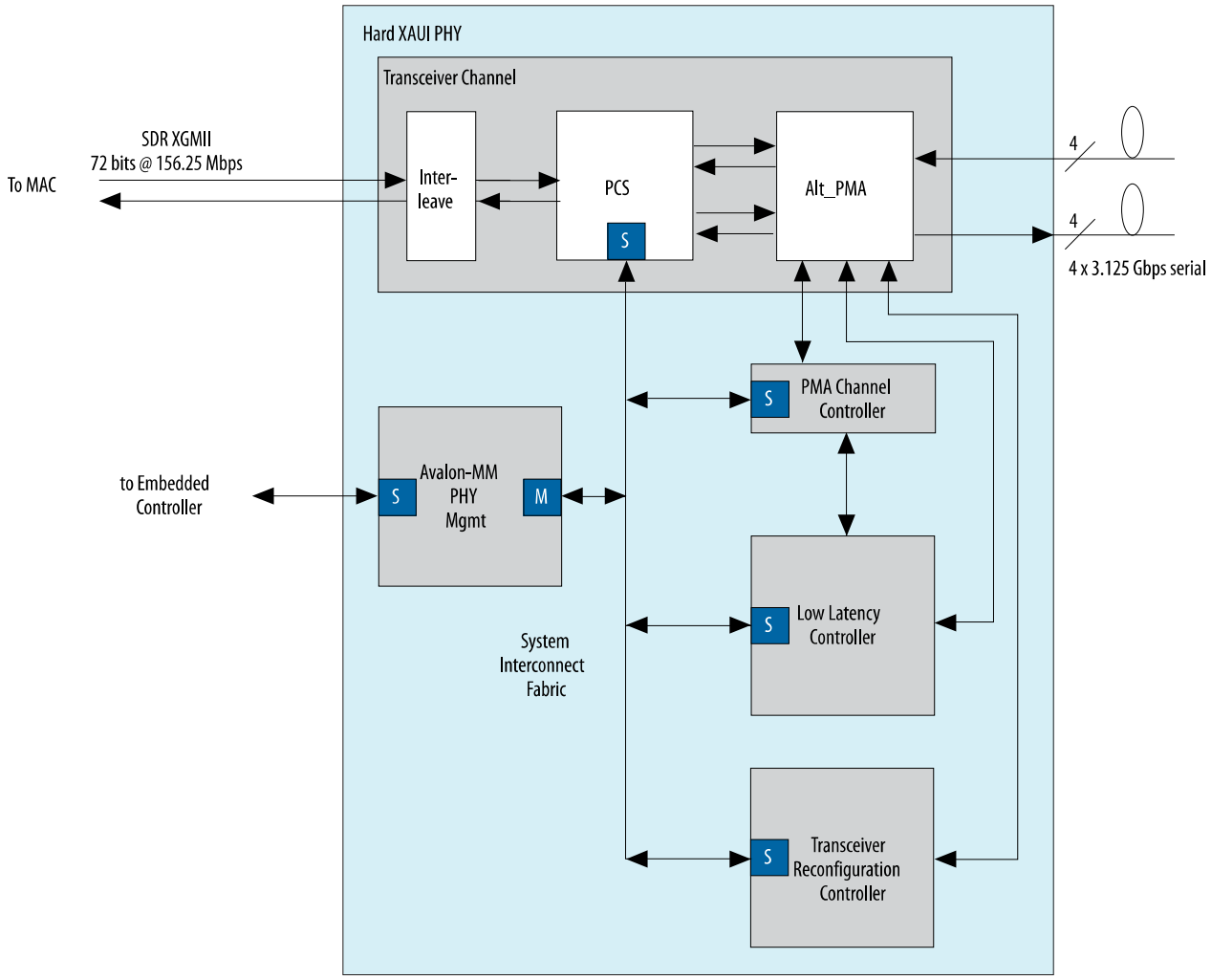
XAUI PHY Configurations

This section describes configurations of the IP core.

The following figure illustrates one configuration of the XAUI IP Core. As this figure illustrates, if your variant includes a single instantiation of the XAUI IP Core, the transceiver reconfiguration control logic is included in the XAUI PHY IP Core. For Arria V, Cyclone V, and Stratix V devices the Transceiver Reconfi-

guration Controller must always be external. Refer to Chapter 16, Transceiver Reconfiguration Controller IP Core for more information about this IP core. The Transceiver Reconfiguration Controller is always separately instantiated in Stratix V and Arria V GZ devices.

Figure 7-2: XAUI PHY with Internal Transceiver Reconfiguration Control



Related Information

Transceiver Reconfiguration Controller IP Core Overview on page 17-1

XAUI PHY Ports

This section describes the ports for the IP core.

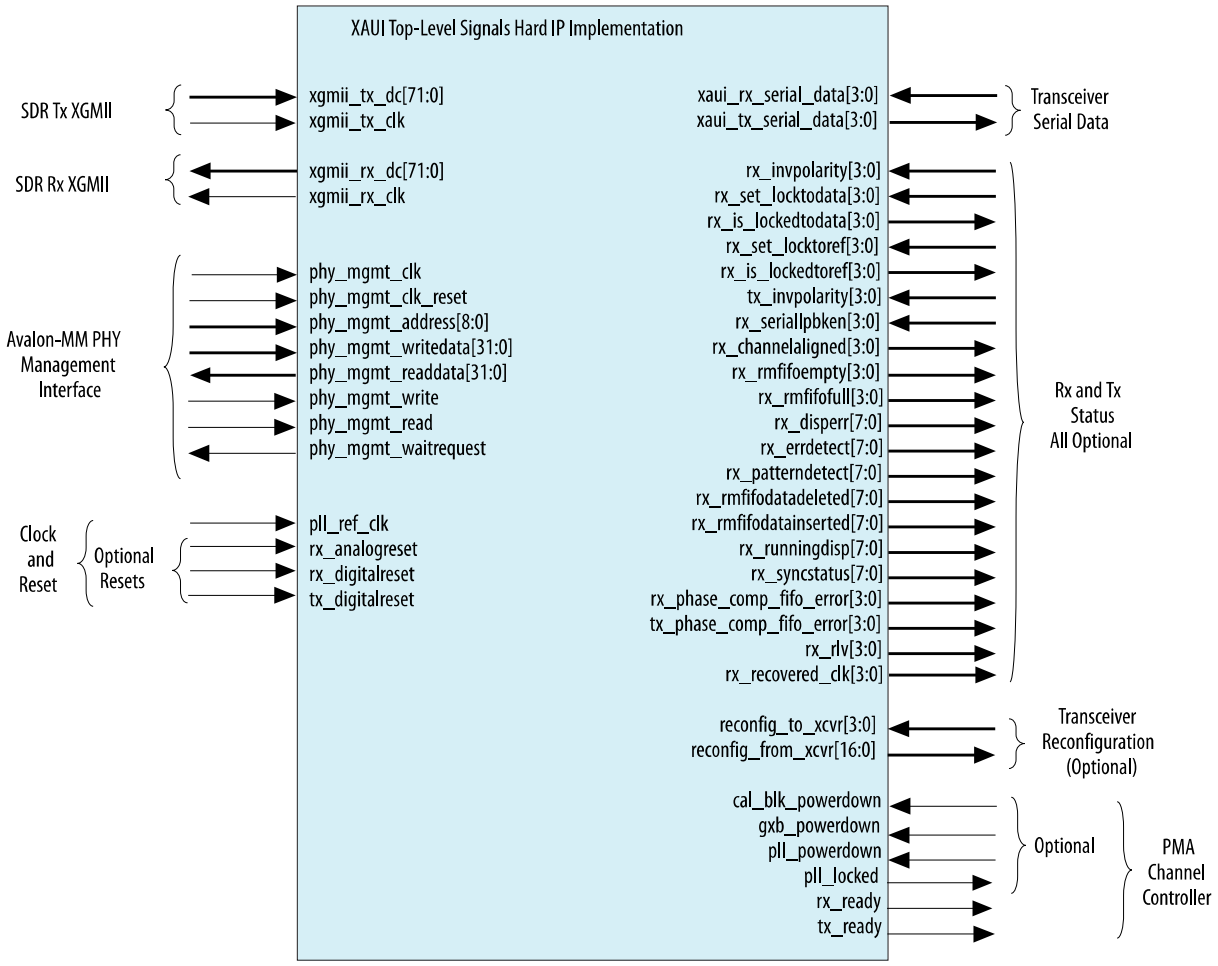
Figure 7-3 illustrates the top-level signals of the XAUI PHY IP Core for the hard IP implementation. This variant is available for Arria II GX, Cyclone IV GX, HardCopy IV and Stratix IV GX devices.**Figure 7-4** illustrates the top-level signals of the XAUI PHY IP Core for the soft IP implementation. With the exception of the optional signals available for debugging and the signals for dynamic reconfiguration of

the transceivers, the top-level signals of the two variants is nearly identical. The DDR XAUI soft IP signals and behavior are the same as the soft IP implementation.

The block diagram shown in the MegaWizard Plug-In Manager GUI labels the external pins with the interface type and places the interface name inside the box. The interface type and name are used to define component interfaces in the **_hw.tcl**. If you turn on Show signals, the block diagram displays all top-level signal names.

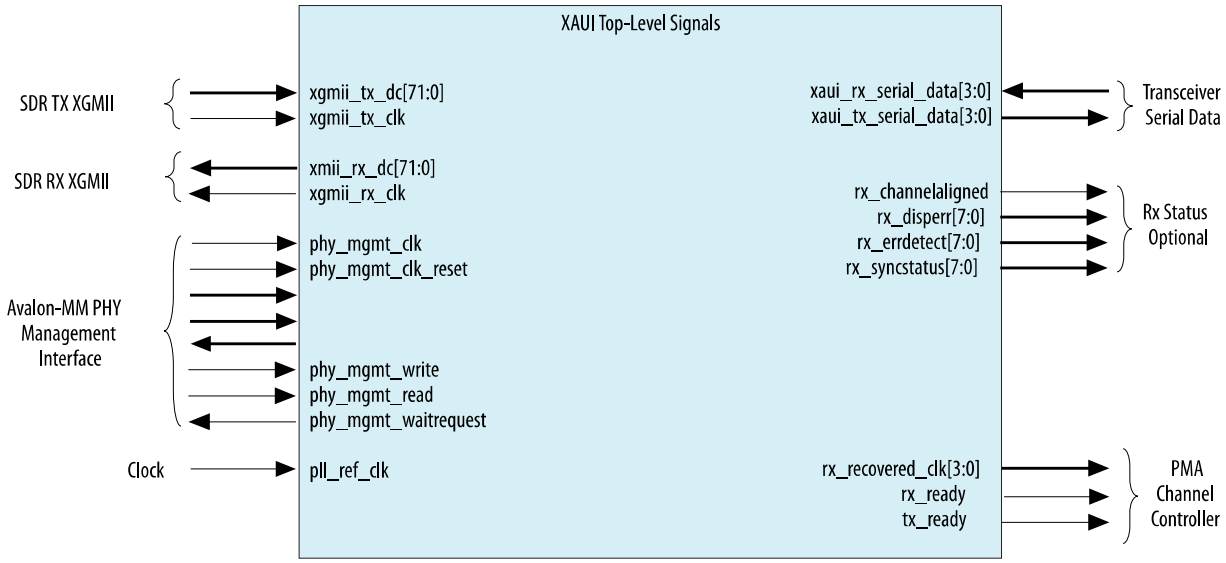
For more information about **_hw.tcl** files refer to refer to the Component Interface Tcl Reference chapter in volume 1 of the Intel Quartus Prime Handbook.

Figure 7-3: XAUI Top-Level Signals–Hard IP PCS and PMA



The following figure illustrates the top-level signals of the XAUI PHY IP Core for the soft IP implementation for both the single and DDR rates.

Figure 7-4: XAUI Top-Level Signals—Soft PCS and PMA



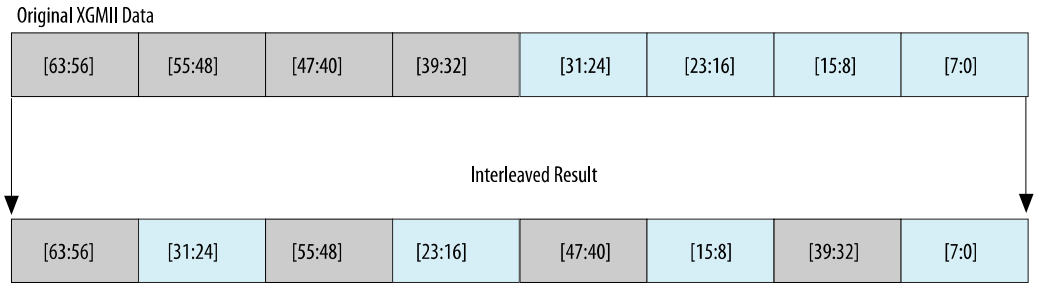
XAUI PHY Data Interfaces

The XAUI PCS interface to the FPGA fabric uses a SDR XGMII interface. This interface implements a simple version of Avalon-ST protocol. The interface does not include ready or valid signals; consequently, the sources always drive data and the sinks must always be ready to receive data.

For more information about the Avalon-ST protocol, including timing diagrams, refer to the *Avalon Interface Specifications*.

Depending on the parameters you choose, the application interface runs at either 156.25 Mbps or 312.5 Mbps. At either frequency, data is only driven on the rising edge of clock. To meet the bandwidth requirements, the datapath is eight bytes wide with eight control bits, instead of the standard four bytes of data and four bits of control. The XAUI IP Core treats the datapath as two, 32-bit data buses and includes logic to interleave them, starting with the low-order bytes.

Figure 7-5: Interleaved SDR XGMII Data Mapping



For the DDR XAUI variant, the start of control character (0xFB) is aligned to either byte 0 or byte 5.

Figure 7-6: Byte 0 Start of Frame Transmission Example

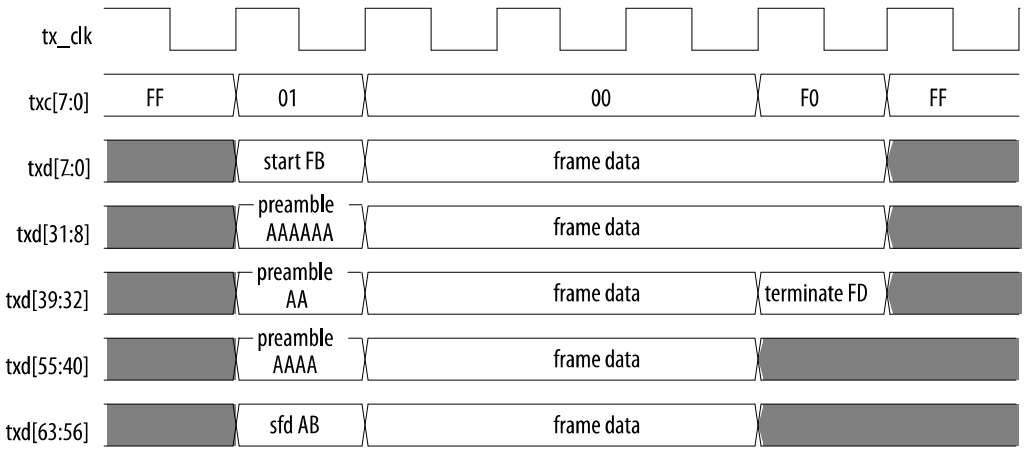
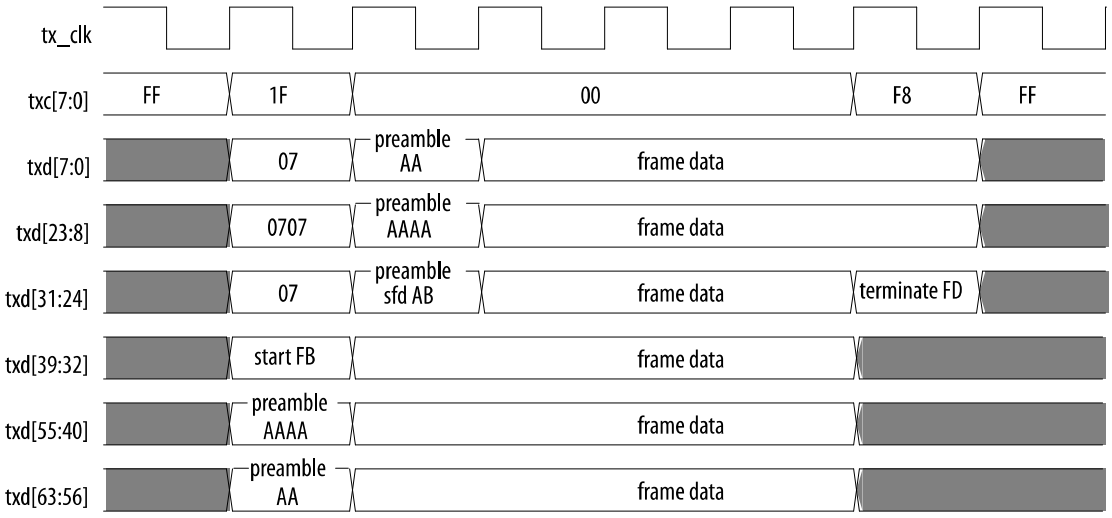


Figure 7-7: Byte 5 Start of Frame Transmission Example



Related Information

Avalon Interface Specifications

SDR XGMII TX Interface

This section describes the signals in the SDR TX XGMII interface.

Table 7-7: SDR TX XGMII Interface

Signal Name	Direction	Description
xgmii_tx_dc[71:0]	Output	Contains 4 lanes of data and control for XGMII. Each lane consists of 16 bits of data and 2 bits of control. • Lane 0–[7:0]/[8], [43:36]/[44] • Lane 1–[16:9]/[17], [52:45]/[53] • Lane 2–[25:18]/[26], [61:54]/[62] • Lane 3–[34:27]/[35],[70:63]/[71]
xgmii_tx_clk	Input	The XGMII SDR TX clock which runs at 156.25 MHz or 312.5 for the DDR variant.

SDR XGMII RX Interface

This section describes the signals in the SDR RX XGMII interface.

Table 7-8: SDR RX XGMII Interface

Signal Name	Direction	Description
xgmii_rx_dc_[71:0]	Input	Contains 4 lanes of data and control for XGMII. Each lane consists of 16 bits of data and 2 bits of control. • Lane 0–[7:0]/[8], [43:36]/[44] • Lane 1–[16:9]/[17], [52:45]/[53] • Lane 2–[25:18]/[26], [61:54]/[62] • Lane 3–[34:27]/[35],[70:63]/[71]
xgmii_rx_clk	Output	The XGMII SDR RX clock which runs at 156.25 MHz.

Transceiver Serial Data Interface

This section describes the signals in the XAUI transceiver serial data interface.

The XAUI transceiver serial data interface has four lanes of serial data for both the TX and RX interfaces. This interface runs at 3.125 GHz or 6.25 GHz depending on the variant you choose. There is no separate clock signal because it is encoded in the data.

Table 7-9: Serial Data Interface

Signal Name	Direction	Description
xaui_rx_serial_data[3:0]	Input	Serial input data.
xaui_tx_serial_data[3:0]	Output	Serial output data.

XAUI PHY Clocks, Reset, and Powerdown Interfaces

This section describes the clocks, reset, and oowerdown interfaces.

Figure 7-8: Clock Inputs and Outputs for IP Core with Hard PCS

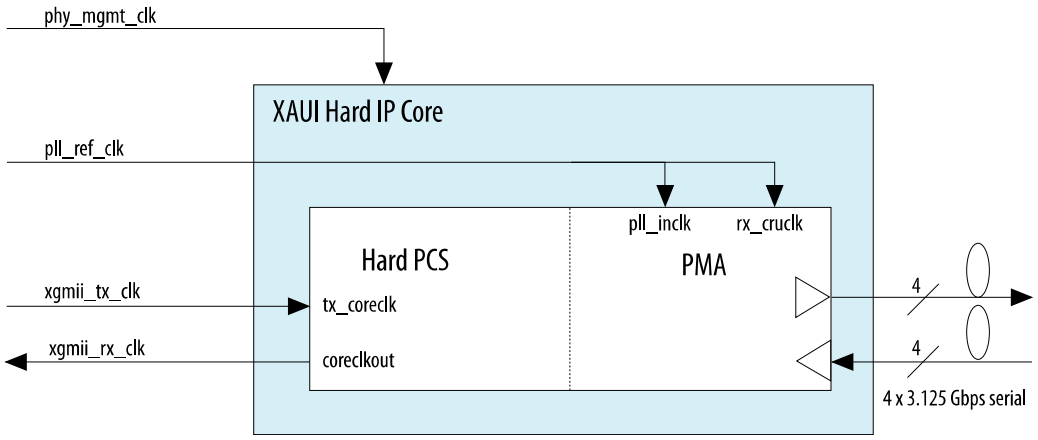


Figure 7-9: Clock Inputs and Outputs for IP Core with Soft PCS

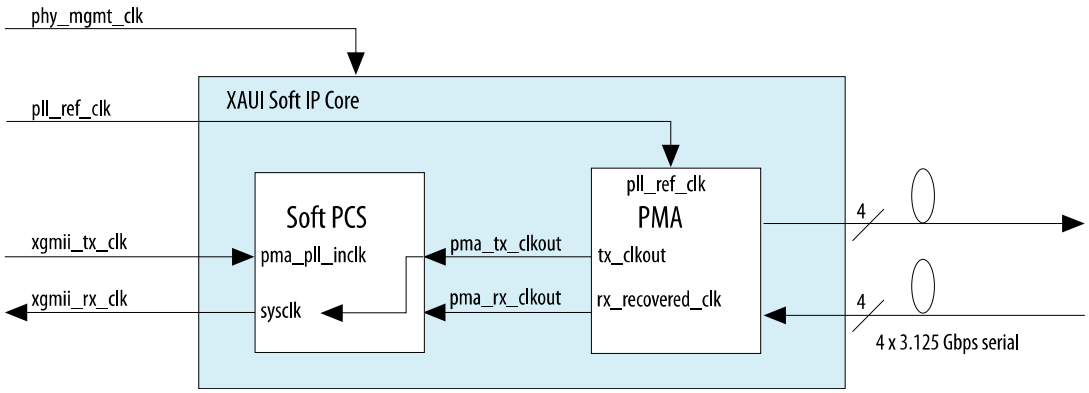


Table 7-10: Optional Clock and Reset Signals

Signal Name	Direction	Description
pll_ref_clk	Input	This is a 156.25 MHz reference clock that is used by the TX PLL and CDR logic.
rx_analogreset	Input	This signal resets the analog CDR and deserializer logic in the RX channel. It is available only for the hard IP implementation.
rx_digitalreset	Input	PCS RX digital reset signal. It is available only for the hard IP implementation.

Signal Name	Direction	Description
tx_digitalreset	Input	PCS TX digital reset signal. If your design includes bonded TX PCS channels, refer to Timing Constraints for Reset Signals when Using Bonded PCS Channels for a SDC constraint you must include in your design. It is available only for the hard IP implementation.
xgmii_tx_clk	Input	The XGMII TX clock which runs at 156.25 MHz. Connect xgmii_tx_clk to xgmii_rx_clk to guarantee this clock is within 150 ppm of the transceiver reference clock.
xgmii_rx_clk	Output	This clock is generated by the same reference clock that is used to generate the transceiver clock. Its frequency is 156.25 MHz. Use this clock for the MAC interface to minimize the size of the FIFO between the MAX and SDR XGMII RX interface.

Refer to Transceiver Reconfiguration Controller for additional information about reset.

Related Information

Transceiver Reconfiguration Controller IP Core Overview on page 17-1

XAUI PHY PMA Channel Controller Interface

This sectiondescribes the signals in the PMA channel controller interface.

Table 7-11: PMA Channel Controller Signals

Signal Name	Direction	Description
cal_blk_powerdown	Input	Powers down the calibration block. A high-to-low transition on this signal restarts calibration. Only available in Arria II GX, HardCopy IV, and Stratix IV GX, and Stratix IV GT devices.
gxb_powerdown	Input	When asserted, powers down the entire transceiver block. Only available in Arria II GX, HardCopy IV, and Stratix IV GX, and Stratix IV GT devices.
pll_powerdown	Input	Powers down the CMU PLL. Only available in Arria II GX, HardCopy IV, and Stratix IV GX, and Stratix IV GT devices.
pll_locked	Output	Indicates CMU PLL is locked. Only available in Arria II GX, HardCopy IV, and Stratix IV GX, and Stratix IV GT devices.
rx_recovered_clk[3:0]	Output	This is the RX clock which is recovered from the received data stream.

Signal Name	Direction	Description
rx_ready	Output	Indicates PMA RX has exited the reset state and the transceiver can receive data.
tx_ready	Output	Indicates PMA TX has exited the reset state and the transceiver can transmit data.

XAUI PHY Optional PMA Control and Status Interface

You can access the state of the optional PMA control and status signals available in the soft IP implementation using the Avalon-MM PHY Management interface to read the control and status registers which are detailed in XAUI PHY IP Core Registers . However, in some cases, you may need to know the instantaneous value of a signal to ensure correct functioning of the XAUI PHY. In such cases, you can include the required signal in the top-level module of your XAUI PHY IP Core.

Table 7-12: Optional Control and Status Signals—Soft IP Implementation

Signal Name	Direction	Description
rx_channelaligned	Output	When asserted, indicates that all 4 RX channels are aligned.
rx_disperr[7:0]	Output	Received 10-bit code or data group has a disparity error. It is paired with rx_errdetect which is also asserted when a disparity error occurs. The rx_disperr signal is 2 bits wide per channel for a total of 8 bits per XAUI link.
rx_errdetect[7:0]	Output	When asserted, indicates an 8B/10B code group violation. It is asserted if the received 10-bit code group has a code violation or disparity error. It is used along with the rx_disperr signal to differentiate between a code violation error, a disparity error, or both. The rx_errdetect signal is 2 bits wide per channel for a total of 8 bits per XAUI link.
rx_syncstatus[7:0]	Output	Synchronization indication. RX synchronization is indicated on the rx_syncstatus port of each channel. The rx_syncstatus signal is 2 bits per channel for a total of 8 bits per hard XAUI link. The rx_syncstatus signal is 1 bit per channel for a total of 4 bits per soft XAUI link.
rx_is_lockedtodata[3:0]	Output	When asserted indicates that the RX CDR PLL is locked to the incoming data.

Signal Name	Direction	Description
rx_is_lockedtoref[3:0]	Output	When asserted indicates that the RX CDR PLL is locked to the reference clock.
tx_clk312_5	Output	This is the clock used for the SDR XGMII interface.

You can access the state of the PMA control and status signals available in the hard IP implementation using the Avalon-MM PHY Management interface to read the control and status registers which are detailed in XAUI PHY IP Core Registers. However, in some cases, you may need to know the instantaneous value of a signal to ensure correct functioning of the XAUI PHY. In such cases, you can include the required signal in the top-level module of your XAUI PHY IP Core.

Table 7-13: Optional Control and Status Signals—Hard IP Implementation, Stratix IV GX Devices

Name	Direction	Description
rx_invpolarity[3:0]	Input	Dynamically reverse the polarity of every bit of the RX data at the input of the word aligner.
rx_set_locktodata[3:0]	Input	Force the CDR circuitry to lock to the received data.
rx_is_lockedtodata[3:0]	Output	When asserted, indicates the RX channel is locked to input data.
rx_set_locktoref[3:0]	Input	Force the receiver CDR to lock to the phase and frequency of the input reference clock.
rx_is_lockedtoref[3:0]	Output	When asserted, indicates the RX channel is locked to input reference clock.
tx_invpolarity[3:0]	Input	Dynamically reverse the polarity the data word input to the serializer in the TX datapath.
rx_seriallpbken	Input	Serial loopback enable. • 1: Enables serial loopback • 0: Disables serial loopback This signal is asynchronous to the receiver. The status of the serial loopback option is recorded by the PMA channel controller, word address 0x061.
rx_channelaligned	Output	When asserted indicates that the RX channel is aligned.
pll_locked	Output	In LTR mode, indicates that the receiver CDR has locked to the phase and frequency of the input reference clock.
rx_rmfifoempty[3:0]	Output	Status flag that indicates the rate match FIFO block is empty (5 words). This signal remains high as long as the FIFO is empty and is asynchronous to the RX datapath.

Name	Direction	Description
rx_rmfifofull[3:0]	Output	Status flag that indicates the rate match FIFO block is full (20 words). This signal remains high as long as the FIFO is full and is asynchronous to the RX data.
rx_disperr[7:0]	Output	Received 10-bit code or data group has a disparity error. It is paired with rx_errdetect which is also asserted when a disparity error occurs. The rx_disperr signal is 2 bits wide per channel for a total of 8 bits per XAUI link.
rx_errdetect[7:0]	Output	Transceiver 8B/10B code group violation or disparity error indicator. If either signal is asserted, a code group violation or disparity error was detected on the associated received code group. Use the rx_disperr signal to determine whether this signal indicates a code group violation or a disparity error. The rx_errdetect signal is 2 bits wide per channel for a total of 8 bits per XAUI link.
rx_patterndetect[7:0]	Output	Indicates that the word alignment pattern programmed has been detected in the current word boundary. The rx_patterndetect signal is 2 bits wide per channel for a total of 8 bits per XAUI link.
rx_rmfifodatadeleted[7:0]	Output	Status flag that is asserted when the rate match block deletes a ||R|| column. The flag is asserted for one clock cycle per deleted ||R|| column.
rx_rmfifodatainserted[7:0]	Output	Status flag that is asserted when the rate match block inserts a ||R|| column. The flag is asserted for one clock cycle per inserted ||R|| column.
rx_runningdisp[7:0]	Output	Asserted when the current running disparity of the 8B/10B decoded byte is negative. Low when the current running disparity of the 8B/10B decoded byte is positive.
rx_syncstatus[7:0]	Output	Synchronization indication. RX synchronization is indicated on the rx_syncstatus port of each channel. The rx_syncstatus signal is 2 bits wide per channel for a total of 8 bits per XAUI link.
rx_phase_comp_fifo_error[3:0]	Output	Indicates a RX phase comp FIFO overflow or underrun condition.
tx_phase_comp_fifo_error[3:0]	Output	Indicates a TX phase compensation FIFO overflow or underrun condition.
rx_rlv[3:0]	Output	Asserted if the number of continuous 1s and 0s exceeds the number that was set in the run-length option. The rx_rlv signal is asynchronous to the RX datapath and is asserted for a minimum of 2 recovered clock cycles.
rx_recovered_clk	Output	This is the RX clock which is recovered from the received data stream.

XAUI PHY Register Interface and Register Descriptions

This section describes the register interface and descriptions for the IP core.

The Avalon-MM PHY management interface provides access to the XAUI PHY IP Core PCS, PMA, and transceiver reconfiguration registers.

Table 7-14: Avalon-MM PHY Management Interface

Signal Name	Direction	Description
phy_mgmt_clk	Input	Avalon-MM clock input. There is no frequency restriction for Stratix V devices; however, if you plan to use the same clock for the PHY management interface and transceiver reconfiguration, you must restrict the frequency range of phy_mgmt_clk to 100–150 MHz to meet the specification for the transceiver reconfiguration clock. For Arria II GX, Cyclone IV GX, HardCopy IV, and Stratix IV GX the frequency range is 37.5–50 MHz.
phy_mgmt_clk_reset	Input	Global reset signal that resets the entire XAUI PHY. This signal is active high and level sensitive.
phy_mgmt_addr[8:0]	Input	9-bit Avalon-MM address.
phy_mgmt_writedata[31:0]	Input	32-bit input data.
phy_mgmt_readdata[31:0]	Output	32-bit output data.
phy_mgmt_write	Input	Write signal. Asserted high.
phy_mgmt_read	Input	Read signal. Asserted high.
phy_mgmt_waitrequest	Output	When asserted, indicates that the Avalon-MM slave interface is unable to respond to a read or write request. When asserted, control signals to the Avalon-MM slave interface must remain constant.

For more information about the Avalon-MM interface, including timing diagrams, refer to the *Avalon Interface Specifications*.

The following table specifies the registers that you can access using the Avalon-MM PHY management interface using word addresses and a 32-bit embedded processor. A single address space provides access to all registers.

Note: Writing to reserved or undefined register addresses may have undefined side effects.

Table 7-15: XAUI PHY IP Core Registers

Word Addr	Bits	R/W	Register Name	Description
PMA Common Control and Status Registers				
0x021	[31:0]	RW	`cal_blk_powerdown`	Writing a 1 to channel <*n*> powers down the calibration block for channel <*n*>. This register is not available for Stratix V devices.
0x022	[31:0]	R	`pma_tx_pll_is_locked`	Bit[P] indicates that the TX CMU PLL (P) is locked to the input reference clock. There is typically one `pma_tx_pll_is_locked` bit per system. This register is not available for Arria V, Arria V GZ, Cyclone V, or Stratix V devices.
Reset Control Registers–Automatic Reset Controller				
0x041	[31:0]	RW	`reset_ch_bitmask`	Bit mask for reset registers at addresses 0x042 and 0x044. The default value is all 1s. Channel <*n*> can be reset when bit<*n*> = 1.
0x042	[1:0]	W	`reset_control`(write)	Writing a 1 to bit 0 initiates a TX digital reset using the reset controller module. The reset affects channels enabled in the `reset_ch_bitmask`. Writing a 1 to bit 1 initiates a RX digital reset of channels enabled in the `reset_ch_bitmask`. This bit self-clears.
		R	`reset_status`(read)	Reading bit 0 returns the status of the reset controller TX ready bit. Reading bit 1 returns the status of the reset controller RX ready bit. This bit self-clears.
Reset Controls –Manual Mode				

Word Addr	Bits	R/W	Register Name	Description
0x044	[31:4,0]	RW	Reserved	It is safe to write 0s to reserved bits.
	[1]	RW	reset_tx_digital	Writing a 1 causes the internal TX digital reset signal to be asserted, resetting all channels enabled in reset_ch_bitmask. You must write a 0 to clear the reset condition.
	[2]	RW	reset_rx_analog	Writing a 1 causes the internal RX analog reset signal to be asserted, resetting the RX analog logic of all channels enabled in reset_ch_bitmask. You must write a 0 to clear the reset condition.
	[3]	RW	reset_rx_digital	Writing a 1 causes the RX digital reset signal to be asserted, resetting the RX digital channels enabled in reset_ch_bitmask. You must write a 0 to clear the reset condition.
PMA Control and Status Registers				
0x061	[31:0]	RW	phy_serial_loopback	Writing a 1 to channel <*n*> puts channel <*n*> in serial loopback mode. For information about pre- or post-CDR serial loopback modes, refer to Loopback Modes.
0x064	[31:0]	RW	pma_rx_set_locktodata	When set, programs the RX CDR PLL to lock to the incoming data. Bit <*n*> corresponds to channel <*n*>.
0x065	[31:0]	RW	pma_rx_set_locktoref	When set, programs the RX CDR PLL to lock to the reference clock. Bit <*n*> corresponds to channel <*n*>.
0x066	[31:0]	RO	pma_rx_is_lockedtodata	When asserted, indicates that the RX CDR PLL is locked to the RX data, and that the RX CDR has changed from LTR to LTD mode. Bit <*n*> corresponds to channel <*n*>.
0x067	[31:0]	RO	pma_rx_is_lockedtoref	When asserted, indicates that the RX CDR PLL is locked to the reference clock. Bit <*n*> corresponds to channel <*n*>.
XAUI PCS				
0x082	[31:4]	-	Reserved	-
	[3:0]	RW	invpolarity[3:0]	Inverts the polarity of corresponding bit on the RX interface. Bit 0 maps to lane 0 and so on. This register is only available in the hard XAUI implementation. **To block**: Word aligner.

Word Addr	Bits	R/W	Register Name	Description
0x083	[31:4]	-	Reserved	-
	[3:0]	RW	`invpolarity[3:0]`	Inverts the polarity of corresponding bit on the TX interface. Bit 0 maps to lane 0 and so on. This register is only available in the hard XAUI implementation. **To block**: Serializer.
0x084	[31:16]	-	Reserved	-
	[15:8]	R	`patterndetect[7:0]`	When asserted, indicates that the programmed word alignment pattern has been detected in the current word boundary. The RX pattern detect signal is 2 bits wide per channel or 8 bits per XAUI link. Reading the value of the `patterndetect` registers clears the bits.This register is only available in the hard XAUI implementation. **From block**: Word aligner.
	[7:0]		`syncstatus[7:0]`	Records the synchronization status of the corresponding bit. The RX sync status register has 2 bits per channel for a total of 8 bits per hard XAUI link. The RX sync status register has 1 bit per channel for a total of 4 bits per soft XAUI link; soft XAUI uses bits 0–3. Reading the value of the `syncstatus` register clears the bits. **From block**: Word aligner.

Word Addr	Bits	R/W	Register Name	Description
0x085	[31:16]	-	Reserved	-
	[15:8]	R	errdetect[7:0]	When set, indicates that a received 10-bit code group has an 8B/10B code violation or disparity error. It is used along with disperr to differentiate between a code violation error, a disparity error, or both. There are 2 bits per RX channel for a total of 8 bits per XAUI link. Reading the value of the errdetect register clears the bits. **From block**: 8B/10B decoder.
	[7:0]		disperr[7:0]	Indicates that the received 10-bit code or data group has a disparity error. When set, the corresponding errdetect bits are also set. There are 2 bits per RX channel for a total of 8 bits per XAUI link. Reading the value of the errdetect register clears the bits **From block**: 8B/10B decoder.
0x086	[31:8]	-	Reserved	-
	[7:4]	R, sticky	phase_comp_fifo_error[3:0]	Indicates a RX phase compensation FIFO overflow or underrun condition on the corresponding lane. Reading the value of the phase_comp_fifo_error register clears the bits. This register is only available in the hard XAUI implementation **From block**: RX phase compensation FIFO.
	[3:0]		rlv[3:0]	Indicates a run length violation. Asserted if the number of consecutive 1s or 0s exceeds the number that was set in the **Runlength check** option. Bits 0-3 correspond to lanes 0-3, respectively. Reading the value of the RLV register clears the bits. This register is only available in the hard XAUI implementation. **From block**: Word aligner.

Word Addr	Bits	R/W	Register Name	Description
0x087	[31:16]	-	Reserved	-
	[15:8]	R, sticky	rmfifodatainserted[7:0]	When asserted, indicates that the RX rate match block inserted a ||R|| column. Goes high for one clock cycle per inserted ||R|| column. Reading the value of the rmfifodatainserted register clears the bits. This register is only available in the hard XAUI implementation. **From block**: Rate match FIFO.
	[7:0]		rmfifodatadeleted[7:0]	When asserted, indicates that the rate match block has deleted an ||R|| column. The flag goes high for one clock cycle per deleted ||R|| column. There are 2 bits for each lane. Reading the value of the rmfifodatadeleted register clears the bits. This register is only available in the hard XAUI implementation. **From block**: Rate match FIFO.
0x088	[31:8]	-	Reserved	-
	[7:4]	R, sticky	rmfifofull[3:0]	When asserted, indicates that rate match FIFO is full (20 words). Bits 0-3 correspond to lanes 0-3, respectively. Reading the value of the rmfifofull register clears the bits. This register is only available in the hard XAUI implementation **From block**: Rate match FIFO.
	[3:0]		rmfifoempty[3:0]	When asserted, indicates that the rate match FIFO is empty (5 words). Bits 0-3 correspond to lanes 0-3, respectively. Reading the value of the rmfifoempty register clears the bits. This register is only available in the hard XAUI implementation **From block**: Rate match FIFO.

Word Addr	Bits	R/W	Register Name	Description
0x089	[31:3]	-	Reserved	-
	[2:0]	R, sticky	phase_comp_fifo_error[2:0]	Indicates a TX phase compensation FIFO overflow or underrun condition on the corresponding lane. Reading the value of the phase_comp_fifo_error register clears the bits. This register is only available in the hard XAUI implementation **From block**: TX phase compensation FIFO.
0x08a	[0]	RW	simulation_flag	Setting this bit to 1 shortens the duration of reset and loss timer when simulating. Altera recommends that you keep this bit set during simulation.

For more information about the individual PCS blocks, refer to the Transceiver Architecture chapters of the appropriate device handbook.

Related Information

- **Loopback Modes** on page 17-59
- **Avalon Interface Specifications**
- **Transceiver Architecture in Arria II Devices**
- **Transceiver Architecture in Arria V Devices**
- **Cyclone IV Transceivers Architecture**
- **Transceiver Architecture in Cyclone V Devices**
- **Transceiver Architecture in HardCopy IV Devices**
- **Transceiver Architecture in Stratix IV Devices**
- **Transceiver Architecture in Stratix V Devices**

XAUI PHY Dynamic Reconfiguration for Arria II GX, Cyclone IV GX, HardCopy IV GX, and Stratix IV GX

The Arria II GX, Cyclone IV GX, HardCopy IV GX, and Stratix IV GX use the ALTGX_RECONFIG Mega function for transceiver reconfiguration.

For more information about the ALTGX_RECONFIG Megafunction, refer to *ALTGX_RECONFIG Megafunction User Guide for Stratix IV Devices* in volume 2 of the *Stratix IV Device Handbook*.

If your XAUI PHY IP Core includes a single transceiver quad, these signals are internal to the core. If your design uses more than one quad, the reconfiguration signals are external.

Table 7-16: Dynamic Reconfiguration Interface Arria II GX, Cyclone IV GX, HardCopy IV GX, and Stratix IV GX devices

Signal Name	Direction	Description
`reconfig_to_xcvr[3:0]`	Input	Reconfiguration signals from the Transceiver Reconfiguration IP Core to the XAUI transceiver.
`reconfig_from_xcvr[<n>:0]`	Output	Reconfiguration signals from the XAUI transceiver to the Transceiver Reconfiguration IP Core. The size of this bus is depends on the device. For the soft PCS in Stratix IV GX and GT devices, <n> = 68 bits. For hard XAUI variants, <n> = 16. For Stratix V devices, the number of bits depends on the number of channels specified. Refer to Chapter 16, Transceiver Reconfiguration Controller IP Core for more information.

Related Information

- **Transceiver Reconfiguration Controller IP Core Overview** on page 17-1
- **ALTGX_RECONFIG Megafunction User Guide for Stratix IV Devices**

XAUI PHY Dynamic Reconfiguration for Arria V, Arria V GZ, Cyclone V and Stratix V Devices

The Arria V, Arria V GZ, Cyclone V, and Stratix V devices use the Transceiver Reconfiguration Controller IP Core for dynamic reconfiguration.

For more information about this IP core, refer to Chapter 16, Transceiver Reconfiguration Controller IP Core.

Each channel and each TX PLL have separate dynamic reconfiguration interfaces. The MegaWizard Plug-In Manager provides informational messages on the connectivity of these interfaces.

Example 7-2: Informational Messages for the Transceiver Reconfiguration Interface

```
PHY IP will require 8 reconfiguration interfaces for connection to the
external reconfiguration controller.Reconfiguration interface offsets 0-3
are connected to the transceiver channels.Reconfiguration interface offsets
4-7 are connected to the transmit PLLs.
```

Although you must initially create a separate reconfiguration interface for each channel and TX PLL in your design, when the Intel Quartus Prime software compiles your design, it reduces the number of reconfiguration interfaces by merging reconfiguration interfaces. The synthesized design typically includes a reconfiguration interface for at least three channels because three channels share an Avalon-MM slave interface which connects to the Transceiver Reconfiguration Controller IP Core. Conversely, you cannot connect the three channels that share an Avalon-MM interface to different Transceiver Reconfiguration Controller IP Cores. Doing so causes a Fitter error. For more information, refer to "Transceiver Reconfiguration Controller to PHY IP Connectivity".

Related Information

- **Transceiver Reconfiguration Controller to PHY IP Connectivity** on page 17-57
- **Transceiver Reconfiguration Controller IP Core Overview** on page 17-1

Logical Lane Assignment Restriction

If you are using ×6 or ×N bonding, transceiver dynamic reconfiguration requires that you assign the starting channel number.

Logical channel 0 should be assigned to either physical transceiver channel 1 or channel 4 of a transceiver bank. However, if you have already created a PCB with a different lane assignment for logical lane 0, you can use the workaround shown in the following example to remove this restriction. This redefines the `pma_bonding_master` parameter using the Intel Quartus Prime Assignment Editor. In this example, the `pma_bonding_master` was originally assigned to physical channel 1. (The original assignment could also have been to physical channel 4.) The to parameter reassigns the `pma_bonding_master` to the PHY IP instance name. You must substitute the instance name from your design for the instance name shown in quotation marks

Example 7-3: Overriding Logical Channel 0 Channel Assignment Restrictions in Stratix V Devices for ×6 or ×N Bonding

```
set_parameter -name pma_bonding_master "\"1\"" -to "<PHY IP instance name>"
```

Related Information

- **Transceiver Reconfiguration Controller to PHY IP Connectivity** on page 17-57
- **Transceiver Reconfiguration Controller IP Core Overview** on page 17-1

XAUI PHY Dynamic Reconfiguration Interface Signals

This section describes the signals in the reconfiguration interface. This interface uses the Avalon-MM PHY Management interface clock.

Table 7-17: Reconfiguration Interface

Signal Name	Direction	Description
`reconfig_to_xcvr [(<n>70)-1:0]`	Input	Reconfiguration signals from the Transceiver Reconfiguration Controller. <*n*> grows linearly with the number of reconfiguration interfaces. <*n*> initially includes the total number transceiver channels and TX PLLs before optimization/merging.
`reconfig_from_xcvr [(<n>46)-1:0]`	Output	Reconfiguration signals to the Transceiver Reconfiguration Controller. <*n*> grows linearly with the number of reconfiguration interfaces. <*n*> initially includes the total number transceiver channels before optimization/merging.

Related Information

- **Transceiver Reconfiguration Controller to PHY IP Connectivity** on page 17-57
- **Transceiver Reconfiguration Controller IP Core Overview** on page 17-1

SDC Timing Constraints

The SDC timing constraints and approaches to identify false paths listed for Stratix V Native PHY IP apply to all other transceiver PHYs listed in this user guide. Refer to *SDC Timing Constraints of Stratix V Native PHY* for details.

Related Information

SDC Timing Constraints of Stratix V Native PHY on page 13-72
This section describes SDC examples and approaches to identify false timing paths.

Simulation Files and Example Testbench

Refer to "Running a Simulation Testbench" for a description of the directories and files that the Intel Quartus Prime software creates automatically when you generate your XAUI PHY IP Core.

Refer to the *Intel FPGA Wiki* for an example testbench that you can use as a starting point in creating your own verification environment.

Related Information

- **Running a Simulation Testbench** on page 1-6
- **Intel FPGA Wiki**